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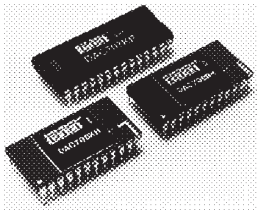


DAC707
DAC708
DAC709

Microprocessor-Compatible 16-BIT DIGITAL-TO-ANALOG CONVERTERS

FEATURES

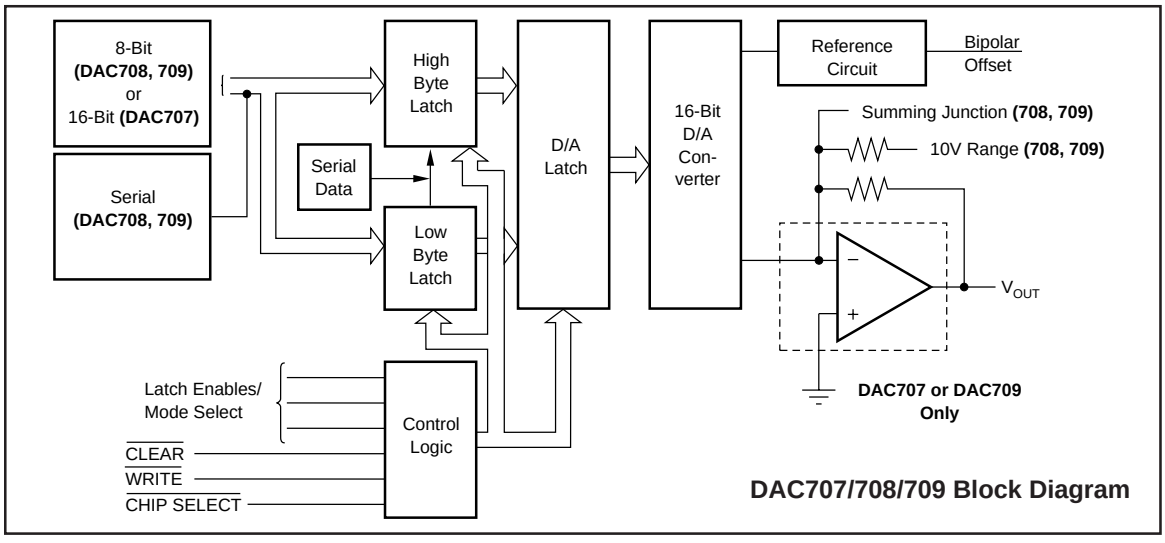
- TWO-CHIP CONSTRUCTION
- HIGH-SPEED 16-BIT PARALLEL, 8-BIT (BYTE) PARALLEL, AND SERIAL INPUT MODES
- DOUBLE-BUFFERED INPUT REGISTER CONFIGURATION
- V_{OUT} AND I_{OUT} MODELS
- HIGH ACCURACY:
  Linearity Error ±0.003% of FSR max
  Differential Linearity Error ±0.006% of FSR max
- MONOTONIC (TO 14 BITS) OVER SPECIFIED TEMPERATURE RANGE
- HERMETICALLY SEALED
- LOW COST PLASTIC VERSIONS AVAILABLE (DAC707JP/KP)

DESCRIPTION

The DAC708 and DAC709 are 16-bit converters designed to interface to an 8-bit microprocessor bus. 16-bit data is loaded in two successive 8-bit bytes into parallel 8-bit latches before being transferred into the D/A latch. The DAC708 and DAC709 are current and voltage output models respectively and are in 24-pin hermetic DIPs. Input coding is Binary Two's Complement (bipolar) or Unipolar Straight Binary (unipolar, when an external logic inverter is used to invert the MSB). In addition, the DAC708/709 can be loaded serially (MSB first).

The DAC707 is designed to interface to a 16-bit bus. Data is written into a 16-bit latch and subsequently the D/A latch. The DAC707 has bipolar voltage output and input coding is Binary Two's Complement (BTC).

All models have Write and Clear control lines as well as input latch enable lines. In addition, DAC708 and DAC709 have Chip Select control lines. In the bipolar mode, the Clear input sets the D/A latch to give zero voltage or current output. They are all 14-bit accurate and are complete with reference, and for the DAC707, and DAC709, a voltage output amplifier. All models are available with an optional burn-in screening.



DAC707/708/709 Block Diagram

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10-minute warm-up, unless otherwise noted.

	DAC707JP			DAC707/708/709KH, DAC707KP			DAC707/708/709BH, SH			
PRODUCT	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT										
DIGITAL INPUT										
Resolution			16			*			*	Bits
Bipolar Input Code (all models)		Binary Two's Complement			*			*		
Unipolar Input Code[1] (DAC708/709 only)					Unipolar Straight Binary			*		
Logic Levels[2]: V_{IH}	+2.0		+5.5	*		*	*		*	V
V_{IL}	–1.0		+0.8	*		*	*		*	V
I_{IH} (V_I = +2.7V)			1			*			*	µA
I_{IL} (V_I = +0.4V)			1			*			*	µA
TRANSFER CHARACTERISTICS										
ACCURACY[3]										
Linearity Error		±0.003	±0.006		±0.0015	±0.003		*	*	% of FSR[4]
Differential Linearity Error[5]		±0.0045	±0.012		±0.003	±0.006		*	*	% of FSR
at Bipolar Zero[5, 6]					±0.003	±0.006		±0.0015	±0.003	% of FSR
Gain Error[7]		±0.07	±0.30		*	±0.15		±0.05	±0.10	%
Zero Error[7]		±0.05	±0.1		*	*		*	*	% of FSR
Monotonicity Over Spec Temp Range	13			14			14			Bits
Power Supply Sensitivity: $+V_{CC}$, $-V_{CC}$		±0.0015	±0.006		*	*		*	±0.003	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001		*	*		*	*	% of FSR/%V_{DD}
DRIFT (Over Spec Temp Range[3])										
Total Error Over Temp Range[8]		±0.08			*	±0.15		*	±0.10	% of FSR
Total Full Scale Drift		±10			*	±25		*	±15	ppm of FSR/°C
Gain Drift		±10	±30		*	±25		±7	±15	ppm/°C
Zero Drift: Unipolar (DAC708/709 only)					±2.5	±5		±1.5	±3	ppm of FSR/°C
Bipolar (all models)		±5	±15		*	±12		±4	±10	ppm of FSR/°C
Differential Linearity Over Temp[5]			±0.012			+0.009, –0.006			*	% of FSR
Linearity Error Over Temp[5]			±0.012			±0.006			*	% of FSR
SETTLING TIME (to ±0.003% of FSR)[9]										
Voltage Output Models										
Full Scale Step (2kΩ load)		4			*	8		*	8	µs
1LSB Step at Worst Case Code[10]		2.5			*	4		*	4	µs
Slew Rate		10			*			*		V/µs
Current Output Models										
Full Scale Step (2mA): 10 to 100Ω Load					350			*		ns
1kΩ Load					1			*		µs
OUTPUT										
VOLTAGE OUTPUT MODELS										
Output Voltage Range										
DAC709: Unipolar (USB Code)					0 to +10			*		V
Bipolar (BTC Code)					±5, ±10			*		V
DAC707 Bipolar (BTC Code)		±10			*			*		V
Output Current	±5			*			*			mA
Output Impedance		0.15			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*		
CURRENT OUTPUT MODELS										
Output Current Range (±30% typ)										
DAC708: Unipolar (USB Code)					0 to –2			*		mA
Bipolar (BTC Code)					±1			*		mA
Unipolar Output Impedance (±30% typ)					4.0			*		kΩ
Bipolar Output Impedance (±30% typ)					2.45			*		kΩ
Compliance Voltage					±2.5			*		V

ELECTRICAL (CONT)

At T_A = +25°C, V_{CC} = ±15V, V_{DD} = +5V, and after a 10-minute warm-up, unless otherwise noted.

PRODUCT	DAC707JP			DAC707/708/709KH, DAC707KP			DAC707/708/ 709BH, SH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS										
Voltage (all models): $+V_{CC}$	+13.5	+15	+16.5	*	*	*	*	*	*	V
$-V_{CC}$	–13.5	–15	–16.5	*	*	*	*	*	*	V
V_{DD}	+4.5	+5	+5.5	*	*	*	*	*	*	V
Current (No Load, +15V Supplies)										
Current Output Models: $+V_{CC}$					+10	+25		*	*	mA
$-V_{CC}$					–13	–25		*	*	mA
V_{DD}					+5	+10		*	*	mA
Voltage Output Models: $+V_{CC}$		+16	+30		*	*		*	*	mA
$-V_{CC}$		–18	–30		*	*		*	*	mA
V_{DD}		+5	+10		*	*		*	*	mA
Power Dissipation (±15V supplies)										
Current Output Models					370	800		*	*	mW
Voltage Output Models		535			*	950		*	*	mW
TEMPERATURE RANGE										
Specification: BH Grades							–25		+85	°C
JP, KP, KH Grades	0		+70	*		*				°C
SH Grades							–55		+125	°C
Storage: Ceramic				–65		+150	–65		+150	°C
Plastic	–60		+100	*		*				°C

*Specification same as for models in column to the left.

NOTES: (1) MSB must be inverted externally prior to DAC708/709 input. (2) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC and 54/74HTC compatible over the specified temperature range. (3) DAC708 (current-output models) are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all tests. (4) FSR means Full Scale Range. For example, for ±10V output, FSR = 20V. (5) ±0.0015% of Full Scale Range is equal to 1 LSB in 16-bit resolution, ±0.003% of Full Scale Range is equal to 1 LSB in 15-bit resolution. ±0.006% of Full Scale Range is equal to 1 LSB in 14-bit resolution. (6) Error at input code 0000_H. (For unipolar connection on DAC708/709, the MSB must be inverted externally prior to D/A input.) (7) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (8) With gain and zero errors adjusted to zero at +25°C. (9) Maximum represents the 3σ limit. Not 100% tested for this parameter. (10) The bipolar worst-case code change is $FFFF_H$ to 0000_H and 0000_H to $FFFF_H$. For unipolar (DAC708/709 only) it is $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
DAC707JP	28-Pin Plastic DBL Wide DIP	215
DAC707KP	28-Pin Plastic DBL Wide DIP	215
DAC707BH	28LD Side Brazed Hermetic Dip	149
DAC707KH	28LD Side Brazed Hermetic DIP	149
DAC707SH	28LD Side Brazed Hermetic DIP	149
DAC708BH	24LD Side Brazed Hermetic DIP	165
DAC708KH	24LD Side Brazed Hermetic DIP	165
DAC708SH	24LD Side Brazed Hermetic DIP	165
DAC709BH	24LD Side Brazed Hermetic DIP	165
DAC709KH	24LD Side Brazed Hermetic DIP	165
DAC709SH	24LD Side Brazed Hermetic DIP	165

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to COMMON	0V, +15V
$+V_{CC}$ to COMMON	0V, +18V
$-V_{CC}$ to COMMON	0V, –18V
Digital Data Inputs to COMMON	–0.5V, V_{DD} +0.5
DC Current any input	±10mA
Reference Out to COMMON	Indefinite Short to COMMON
V_{OUT} (DAC707, DAC709)	Indefinite Short to COMMON
External Voltage Applied to R_F (pin 13 or 14, DAC708)	±18V
External Voltage Applied to D/A Output (pin 1, DAC707; pin 14, DAC709)	±5V
Power Dissipation	1000mW
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

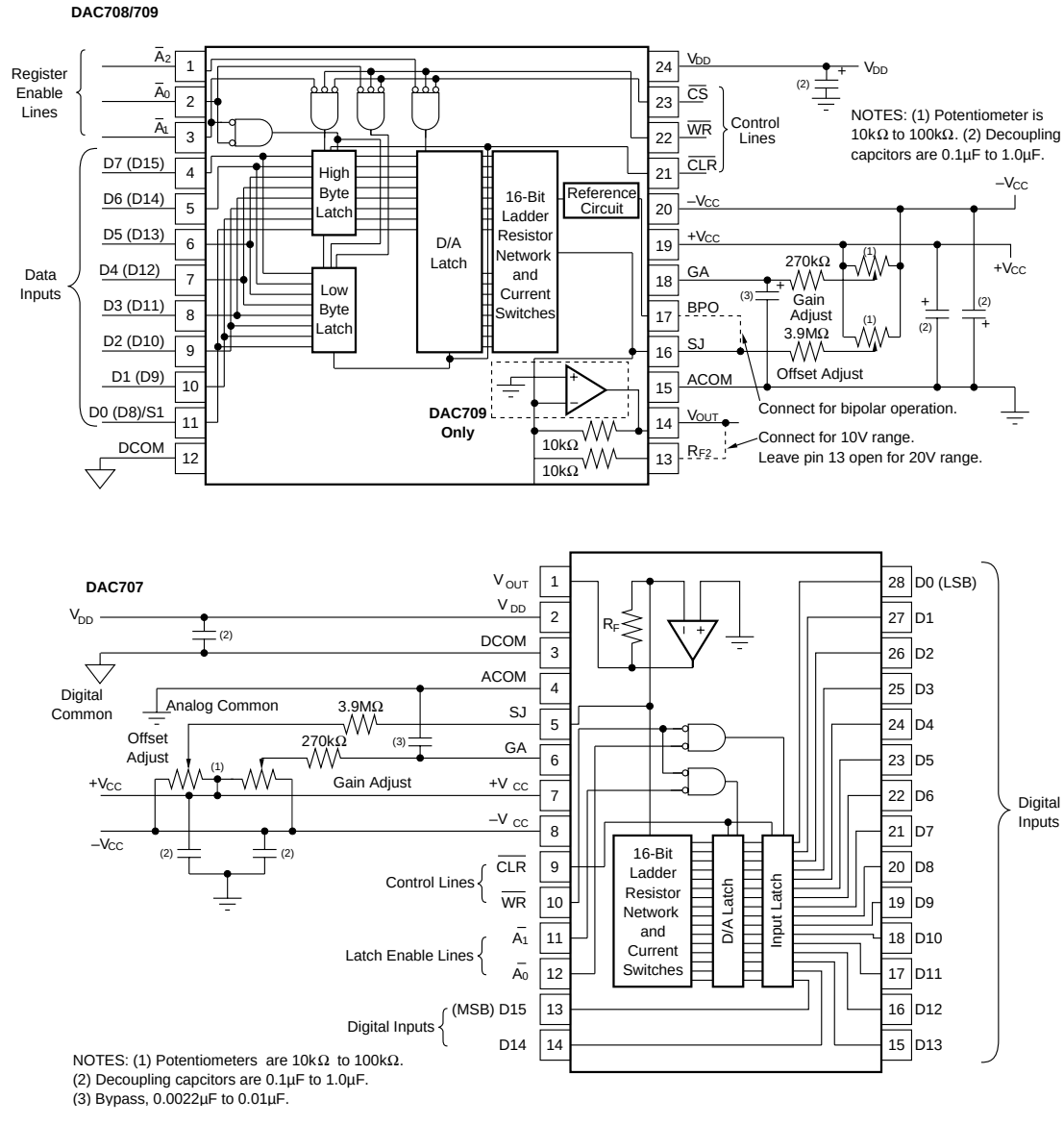
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	TEMPERATURE RANGE	INPUT CONFIGURATION	OUTPUT CONFIGURATION
DAC707JP	0°C to +70°C	16-bit port	±10V output
DAC707JP-BI[1]	0°C to +70°C	16-bit port	±10V output
DAC707KP	0°C to +70°C	16-bit port	±10V output
DAC707KP-BI[1]	0°C to +70°C	16-bit port	±10V output
DAC707KH	0°C to +70°C	16-bit port	±10V output
DAC707KH-BI[1]	0°C to +70°C	16-bit port	±10V output
DAC707BH	–25°C to +85°C	16-bit port	±10V output
DAC707BH-BI[1]	–25°C to +85°C	16-bit port	±10V output
DAC707SH	–55°C to +125°C	16-bit port	±10V output
DAC707SH-BI[1]	–55°C to +125°C	16-bit port	±10V output
DAC708KH	0°C to +70°C	8-bit port	±1mA output
DAC708BH	–25°C to +85°C	8-bit port	±1mA output
DAC708SH	–55°C to +125°C	8-bit port	±1mA output
DAC709KH	0°C to +70°C	8-bit port	±10V output
DAC709BH	–25°C to +85°C	8-bit port	±10V output
DAC709SH	–55°C to +125°C	8-bit port	±10V output

NOTE: (1) 25 piece minimum order.

CONNECTION DIAGRAMS



DESCRIPTION OF PIN FUNCTIONS

DAC707		Pin	DAC708/709	
DESIGNATOR	**DESCRIPTION**	**#**	**DESIGNATOR**	**DESCRIPTION**
V_{OUT}	Voltage output for DAC707 (±10V)	1	A_2	Latch enable for D/A latch (Active low)
V_{DD}	Logic supply (+5V)	2	A_0	Latch enable for "low byte" input (Active low). When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled.
DCOM	Digital common	3	A_1	Latch enable for "high byte" input (Active low). When both A_0 and A_1 are logic "0", the serial input mode is selected and the serial input is enabled.
ACOM	Analog common	4	D7 (D15)	Input for data bit 7 if enabling low byte (LB) latch or data bit 15 if enabling the high byte (HB) latch.
SJ	Summing junction of the internal output op amp for the DAC707. Offset adjust circuit is connected to the summing junction of the output amplifier. Refer to Block Diagram.	5	D6 (D14)	Input for data bit 6 if enabling LB latch or data bit 14 if enabling the HB latch.
GA	Gain adjust pin. Refer to Connection Diagram for gain adjust circuit.	6	D5 (D13)	Data bit 5 (LB) or data bit 13 (HB)
$+V_{CC}$	Positive supply voltage (+15V)	7	D4 (D12)	Data bit 4 (LB) or data bit 12 (HB)
$-V_{CC}$	Negative supply voltage (–15V)	8	D3 (D11)	Data bit 3 (LB) or data bit 11 (HB)
$\overline{CLR}$	Clear line. Sets the input latch to zero and sets the D/A latch to the input code that gives bipolar zero on the D/A output (Active low)	9	D2 (D10)	Data bit 2 (LB) or data bit 10 (HB)
$\overline{WR}$	Write control line (Active low)	10	D1 (D9)	Data bit 1 (LB) or data bit 9 (HB)
$\overline{A_1}$	Enable for D/A converter latch (Active low)	11	D0 (D8)/SI	Data bit 0 (LB) or data bit 8 (HB). Serial input when serial mode is selected.
$\overline{A_0}$	Enable for input latch (Active low)	12	DCOM	Digital common
D15 (MSB)	Data bit 15 (Most Significant Bit)	13	R_{F2}	Feedback resistor for internal or external operational amplifier. Connect to pin 14 when a 10V output range is desired. Leave open for a 20V output range.
D14	Data bit 14	14	V_{OUT} R_{F1} (DAC708)	Voltage output for DAC709 or feedback resistor for use with an external output op amp for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D13	Data bit 13	15	ACOM	Analog common
D12	Data bit 12	16	SJ (DAC709) I_{OUT} (DAC708)	Summing junction of the internal output op amp for the DAC709, or the current output for the DAC708. Refer to Connection Diagram for connection of external op amp to DAC708.
D11	Data bit 11	17	BPO	Bipolar offset. Connect to pin 16 when operating in the bipolar mode. Leave open for unipolar mode.
D10	Data bit 10	18	GA	Gain adjust pin
D9	Data bit 9	19	$+V_{CC}$	Positive supply voltage (+15V)
D8	Data bit 8	20	$-V_{CC}$	Negative supply voltage (–15V)
D7	Data bit 7	21	$\overline{CLR}$	Clear line. Sets the high and low byte input registers to zero and, for bipolar operation, sets the D/A register to the input code that gives bipolar zero on the D/A output. (In the unipolar mode, invert the MSB prior to the D/A.)
D6	Data bit 6	22	$\overline{WR}$	Write control line
D5	Data bit 5	23	$\overline{CS}$	Chip select control line
D4	Data bit 4	24	V_{DD}	Logic supply (+5V)
D3	Data bit 3	25	No pin	
D2	Data bit 2	26	No pin	(The DAC708 and DAC709 are in 24-pin packages)
D1	Data bit 1	27	No pin	
D0 (LSB)	Data bit 0 (Least Significant Bit)	28	No pin	

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

For bipolar operation, the DAC707/708/709 accept positive-true binary two's complement input code. For unipolar operation (DAC708/709 only) the input code is positive-true straight-binary provided that the MSB input is inverted with an external inverter. See Table I.

Digital Input Codes	ANALOG OUTPUT	
	Unipolar Straight Binary(1) (DAC708/709 only; connected for Unipolar operation)	Binary Two's Complement (Bipolar operation; all models)
$7FFF_H$	+1/2 Full Scale –1LSB(2)	+Full Scale
0000_H	Zero	Zero
$FFFF_H$	+Full Scale	–1LSB
8000_H	+1/2 Full Scale	–Full Scale
NOTES: (1) MSB must be inverted externally. (2) Assumes MSB is inverted externally.		

TABLE I. Digital Input Codes.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (–Full Scale point and +Full Scale point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of ±1/2LSB means that the output step size can be between 1/2LSB and 3/2LSB when the input changes between adjacent codes. A negative DLE specification of –1LSB maximum (–0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC707/708/709 are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain Drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by: (1) testing the end point differences at t_{MIN}, +25°C and t_{MAX}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Zero Drift

Zero Drift is a measure of the change in the output with 0000_H applied to the D/A converter inputs over the specified temperature range. (For the DAC708/709 in unipolar mode, the MSB must be inverted). This code corresponds to zero volts (DAC707 and DAC709) or zero milliamps (DAC708) at the analog output. The maximum change in offset at t_{MIN} or t_{MAX} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in FSR/°C.

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

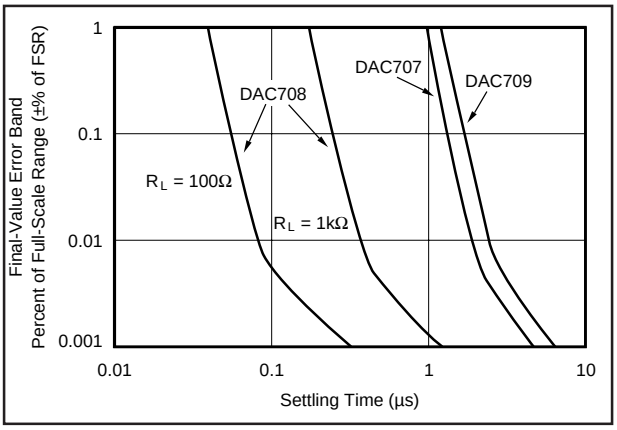


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (±10V) or 10V (±5V or 0 to 10V) and a 1LSB change at the "major carry", the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next.)

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter

output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

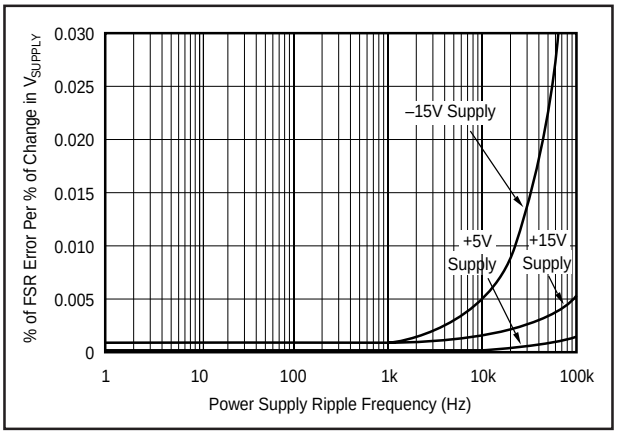


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. 1µF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ resistor. A 0.001µF to 0.01µF ceramic capacitor should be connected from GAIN ADJUST to ANALOG COMMON to prevent noise pickup. Refer to Figures 4 and 5 for the relationship of zero and gain adjustments to unipolar D/A converters.

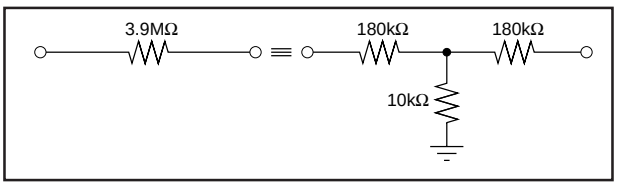


FIGURE 3. Equivalent Resistances.

Zero Adjustment

For unipolar (USB) configurations, apply the digital input code that produces zero voltage or zero current output and adjust the zero potentiometer for zero output.

For bipolar (BTC) configurations, apply the digital input code that produces zero output voltage or current. See Table II for corresponding codes and connection diagrams for zero adjustments circuit connections. Zero calibration should be made before gain calibration.

Gain Adjustment

Apply the digital input that gives the maximum positive output voltage. Adjust the gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages and the Connection Diagrams for gain adjustment circuit connections.

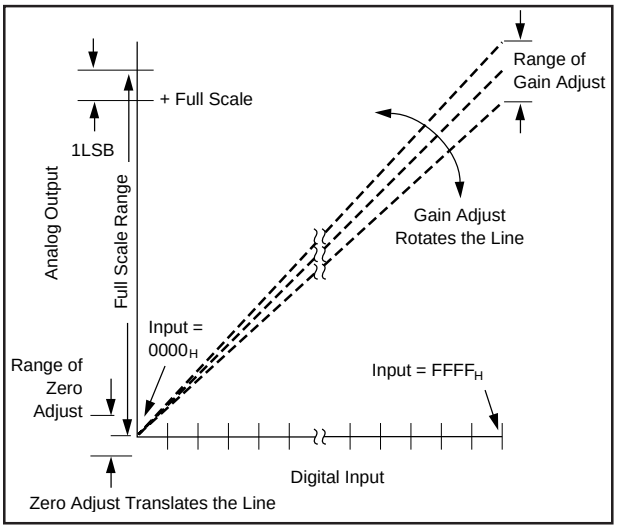


FIGURE 4. Relationship of Zero and Gain Adjustments for Unipolar D/A Converters, DAC708 and DAC709.

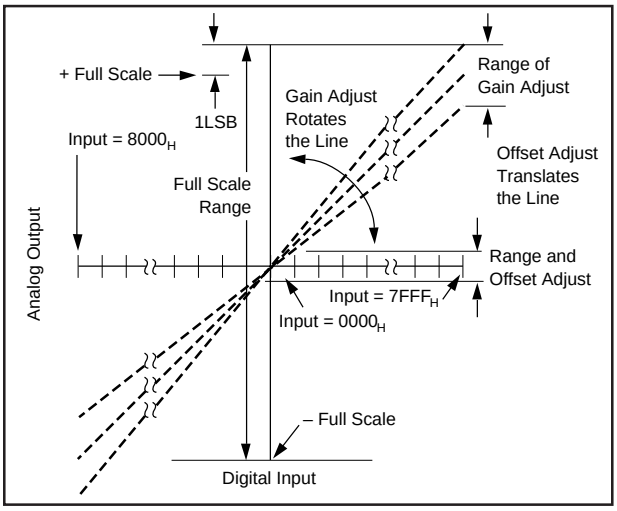


FIGURE 5. Relationship of Zero and Gain Adjustments for Bipolar D/A Converters, DAC707 and DAC708/709

VOLTAGE OUTPUT MODELS												
Digital Input Code	Analog Output Unipolar, 0 to +10V(1)			Units	Digital Input Code	Analog Output Bipolar, ±10V			Analog Output Bipolar, ±5V			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	16-Bit	15-Bit	14-Bit	
One LSB	153	305	610	µV	One LSB	305	610	1224	153	305	610	µV
$FFFF_H$	+9.99985	+9.99969	+9.99939	V	7FFFH	+9.99960	+9.99939	+9.99878	+4.99980	+4.99970	+4.99939	V
0000_H	0	0	0	V	8000H	–10.0000	–10.0000	–10.0000	–5.0000	–5.0000	–5.0000	V

CURRENT OUTPUT MODELS									
Digital Input Code	Analog Output Unipolar, 0 to –2mA(1)			Units	Digital Input Code	Analog Output Bipolar, ±1mA			Units
	16-Bit	15-Bit	14-Bit			16-Bit	15-Bit	14-Bit	
One LSB	0.031	0.061	0.122	µA	One LSB	0.031	0.061	0.122	µA
$FFFF_H$	–1.99997	–1.99994	–1.99988	mA	$7FFF_H$	–0.99997	–0.99994	–0.99988	mA
0000_H	0	0	0	mA	8000_H	+1.00000	+1.00000	+1.00000	mA

NOTE: (1) MSB assumed to be inverted externally.

TABLE II. Digital Input and Analog Output Voltage/Current Relationships.

INTERFACE LOGIC AND TIMING

DAC708/709

The signals CHIP SELECT ($\overline{CS}$), WRITE ($\overline{WR}$), register enables ($\overline{A}_0$, $\overline{A}_1$, and $\overline{A}_2$) and CLEAR ($\overline{CLR}$), provide the control functions for the microprocessor interface. They are all active in the "low" or logic "0" state. $\overline{CS}$ must be low to access any of the registers. $\overline{A}_0$ and $\overline{A}_1$ steer the input 8-bit data byte to the low- or high-byte input latch respectively. $\overline{A}_2$ gates the contents of the two input latches through to the D/A latch in parallel. The contents are then applied to the input of the D/A converter. When $\overline{WR}$ goes low, data is strobed into the latch or latches which have been enabled.

The serial input mode is activated when both $\overline{A}_0$ and $\overline{A}_1$ are logic "0" simultaneously. The D0 (D8)/SI input data line accepts the serial data MSB first. Each bit is clocked in by a $\overline{WR}$ pulse. Data is strobed through to the D/A latch by $\overline{A}_2$ going to logic "0" the same as in the parallel input mode.

Each of the latches can be made "transparent" by maintaining its enable signal at logic "0". However, as stated above, when both $\overline{A}_0$ and $\overline{A}_1$ are logic "0" at the same time, the serial mode is selected.

The $\overline{CLR}$ line resets both input latches to all zeros and sets the D/A latch to 0000_H. This is the binary code that gives a null, or zero, at the output of the D/A in the bipolar mode. In the unipolar mode, activating $\overline{CLR}$ will cause the output to go to one-half of full scale.

The maximum clock rate of the latches is 10MHz. The minimum time between write ($\overline{WR}$) pulses for successive enables is 20ns. In the serial input mode (DAC708 and DAC709), the maximum rate at which data can be clocked into the input shift register is 10MHz.

The timing of the control signals is given in Figure 6.

DAC707

The DAC707 interface timing is the same as that described above except instead of two 8-bit separately-enabled input latches, it has a single 16-bit input latch enabled by $\overline{A}_0$. The D/A latch is enabled by $\overline{A}_1$. Also, there is no serial-input mode and no CHIP SELECT ($\overline{CS}$) line.

LOGIC TIMING - Parallel or Serial Data Input Over Temperature

		ns, min	ns, max
T_{DW}	Data valid to end of $\overline{WR}$	80	
T_{CW}	$\overline{CS}$ valid to end of $\overline{WR}$	80	
T_{AW}	$\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$ valid to end of $\overline{WR}$	80	
T_{WP}	Write pulse width	80	
T_{DH}	Data hold after end of $\overline{WR}$	0	

TIMING DIAGRAM

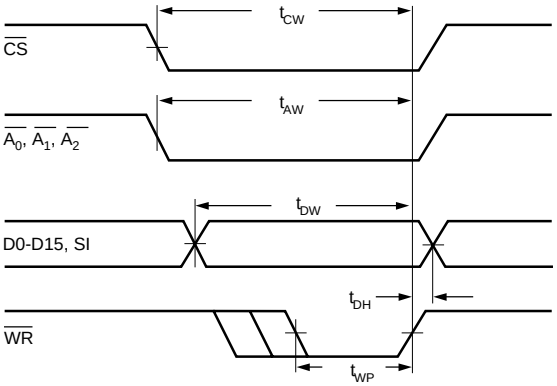


FIGURE 6. Logic Timing Diagram.

INSTALLATION CONSIDERATIONS

Due to the extremely-high accuracy of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153µV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of typical 1 ounce copper-clad printed circuit board material is approximately 1/2mΩ per square. In the example above, a 10 milliinch-wide conductor 60 milliinches long would cause a 1LSB error.

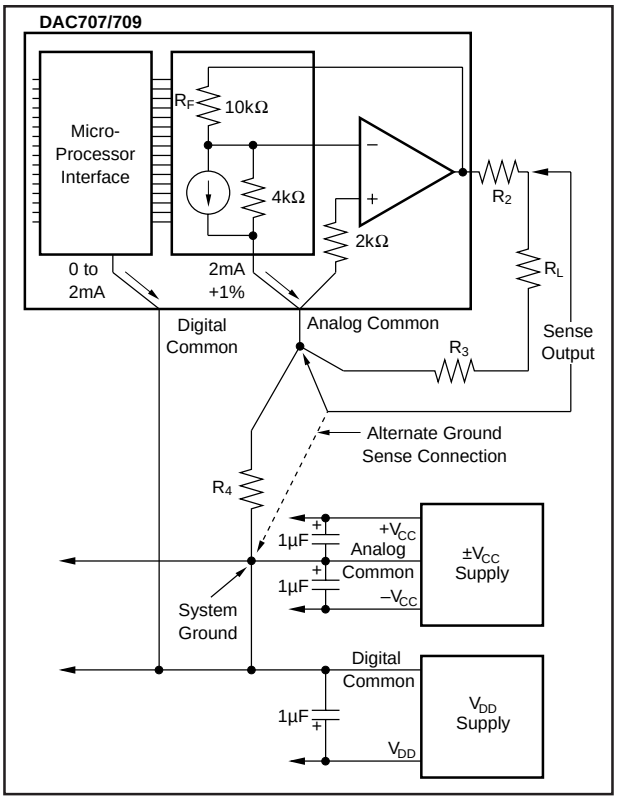


FIGURE 7. DAC707/709 Bipolar Output Circuit (Voltage Out).

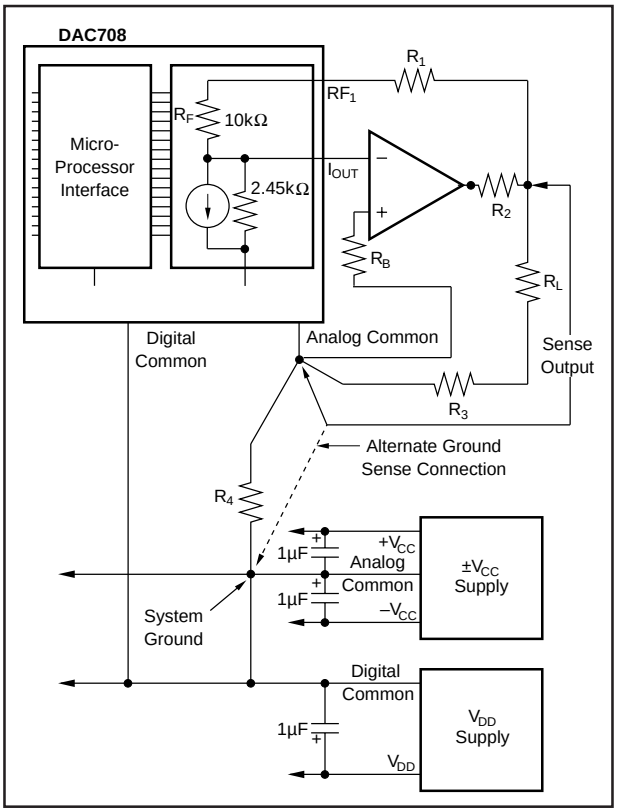


FIGURE 8. DAC708 Bipolar Output Circuit (with External Op Amp).

In Figures 7 and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2 simply introduces a gain error and can be removed with gain calibration. R_3 is part of R_L if the output voltage is sensed at ANALOG COMMON.

Figures 8 and 9 show two methods of connecting the current output model with an external precision output op amp. By sensing the output voltage at the load resistor (connecting R_F to the output of the amplifier at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

In many applications it is impractical to sense the output voltage at ANALOG COMMON. Sensing the output voltage at the system ground point is permissible because these converters have separate analog and digital common lines and the analog return current is a near-constant 2mA and varies by only 10µA to 20µA over the entire input code range. R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 is constant and appears as a zero error that can be nulled with the zero calibration adjustment.

Another approach senses the output at the load as shown in Figure 9. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection across R_L. The effect of R_4 is negligible as explained previously.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small flux-capture cross section for any external field.

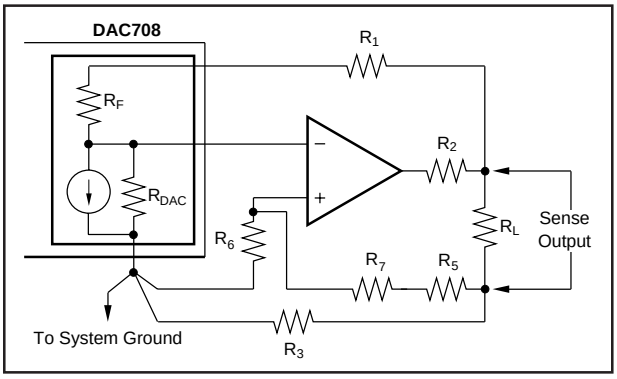


FIGURE 9. Alternate Connection for Ground Sensing at the Load (Current Output Models).

BURN-IN SCREENING

Burn-in screening is an option available for the DAC707. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Product	Temp. Range	Burn-In Screening
DAC707JP-BI	0°C to 70°C	100°C
DAC707KP-BI	0°C to 70°C	100°C
DAC707KH-BI	–25°C to +85°C	125°C
DAC707BH-BI	–25°C to +85°C	125°C
DAC707SH-BI	–55°C to +125°C	125°C

All units are tested after burn-in to ensure that grade specifications are met.

APPLICATIONS

LOADING THE DAC709 SERIALLY ACROSS AN ISOLATION BARRIER

A very useful application of the DAC709 is in achieving low-cost isolation that preserves high accuracy. Using the serial input feature of the input register pair, only three signal lines need to be isolated. The data is applied to pin 11 in a serial bit stream, MSB first. The $\overline{WR}$ input is used as a data strobe, clocking in each data bit. A RESET signal is provided for system startup and reset. These three signals are each optically isolated. Once the 16 bits of serial data have been strobed into the input register pair, the data is strobed through to the D/A register by the "carry" signal out of a 4-bit binary synchronous counter that has counted the 16 $\overline{WR}$ pulses used to clock in the data. The circuit diagram is given in Figure 10.

CONNECTING MULTIPLE DAC707s TO A 16-BIT MICROPROCESSOR BUS

Figure 11 illustrates the method of connecting multiple DAC707s to a 16-bit microprocessor bus. The circuit shown has two DAC707s and uses only one address line to select either the input register or the D/A register. An external address decoder selects the desired converter.

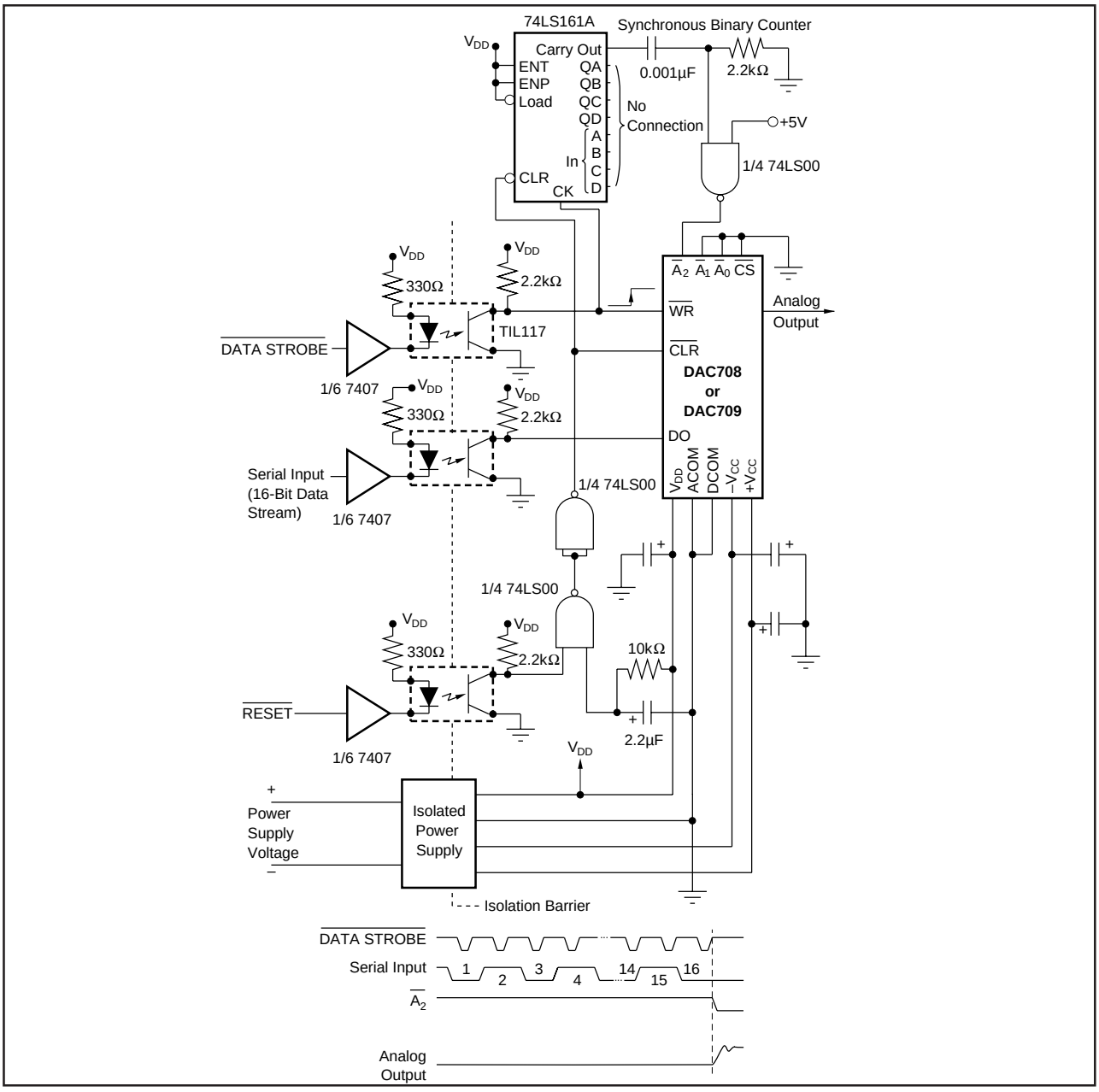


FIGURE 10. Serial Loading of Electrically Isolated DAC708/709.

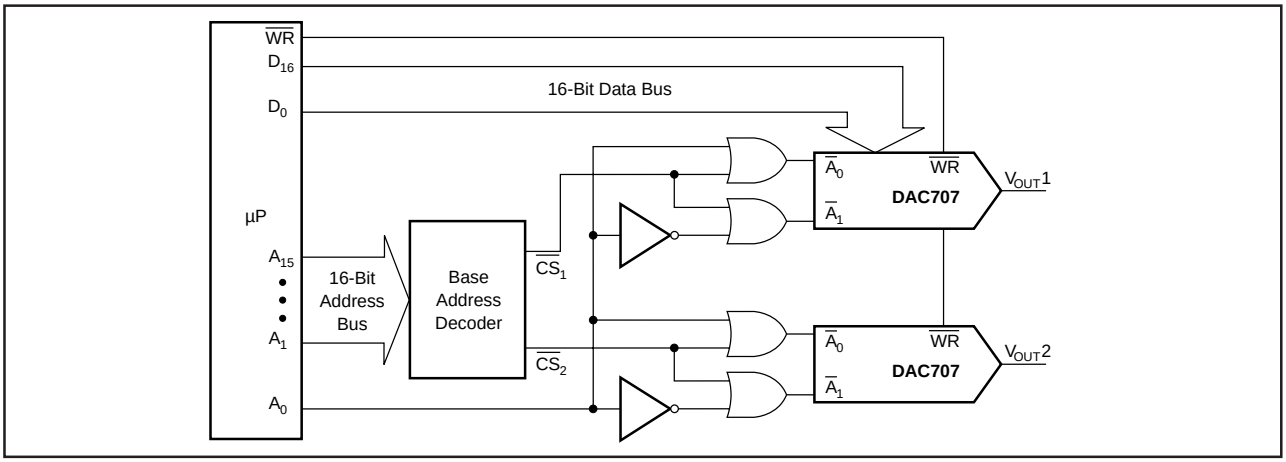


FIGURE 11. Connecting Multiple DAC707s to a 16-Bit Microprocessor.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC707JP	NRND	PDIP	NTD	28	13	TBD	CU SNPB	N / A for Pkg Type
DAC707JP-BI	OBSOLETE	PDIP	NTD	28		TBD	Call TI	Call TI
DAC707KP	NRND	PDIP	NTD	28	13	TBD	CU SNPB	N / A for Pkg Type
DAC707KP-5	OBSOLETE	PDIP	NTD	28		TBD	Call TI	Call TI
DAC707KP-7	OBSOLETE	PDIP	NTD	28		TBD	Call TI	Call TI
DAC707KP-BI	OBSOLETE	PDIP	NTD	28		TBD	Call TI	Call TI
DAC709KH	OBSOLETE	CDIP SB	JDM	24		TBD	Call TI	Call TI
DAC709KH-2	OBSOLETE	CDIP SB	JDM	24		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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